READ FREE DIGITAL CIRCUITS AND DESIGN 3E BY ARIVAZHAGAN S SALIVAHANAN

Book Review | Digital Circuits and Design by Salivahanan | Digital Electronics book for Engineering - Book Review | Digital Circuits and Design by Salivahanan | Digital Electronics book for Engineering by Dr. Sajal Sasmal 3,418 views 4 years ago 6 minutes, 35 seconds - ONLINE TUITION available for any electronics related subjects of Diploma, B.Tech, M.Tech, BCA, MCA, BSc, MSc students for ...
Solving the definite integral using Beta/Gamma functions and Euler's reflection formula - Solving the definite integral using Beta/Gamma functions and Euler's reflection formula by Cipher 411 views 1 day ago 2 minutes, 47 seconds - Mis-2424 Integrate (sin^8 x cos^4 x)^(1/3) dx from 0 to ?/2 #calculus #definite_integrals #betafunction #gammafunction #euler ...
Design of Digital Circuits - Lecture 9: Von Neumann Model, ISA, LC-3, MIPS (ETH Zürich, Spring 2018) - Design of Digital Circuits - Lecture 9: Von Neumann Model, ISA, LC-3, MIPS (ETH Zürich, Spring 2018) by Onur Mutlu Lectures 3,477 views 6 years ago 1 hour, 30 minutes - Design, of **Digital Circuits**,, ETH Zürich, Spring 2018 (https://safari.ethz.ch/digitaltechnik/spring2018/doku.php?id=schedule) ...
Readings
Basic Elements of Computer
Byte-Addressable Memory
Big Endian vs Little Endian
Accessing Memory: MAR and MDR
Processing Unit
Registers
MIPS Register File
Input and Output
Programmer Visible (Architectural) State
LC-3: A Von Neumann Machine
Stored Program \u0026 Sequential Execution
A Sample Program Stored in Memory
Instruction Types
An Example of Operate Instruction
From Assembly to Machine Code in LC-3
From Assembly to Machine Code in MIPS
Instruction Formats: R-Type in MIPS
Reading Operands from Memory
Reading Word-Addressable Memory
Load Word in LC-3 and MIPS
Load Word in Byte-Addressable MIPS
Instruction Format With Immediate
How are these Instructions Executed
The Instruction Cycle
DECODE in LC-3
EVALUATE ADDRESS in LC-3
FETCH OPERANDS in LC-3
STORE RESULT in LC-3
ES3-3- \"ADC-based Wireline Transceivers\" - Yohan Frans - ES3-3- \"ADC-based Wireline Transceivers\" - Yohan Frans by IEEE Solid-State Circuits Society 20,931 views 4 years ago 1 hour, 31 minutes - Abstract: The emergence of PAM4 electrical signaling standard at 56Gb/**s**, and 112Gb/**s**, has caused wider adoption of

ADC-based ...
56Gb/s PAM4 vs NRZ Over Legacy Channel
Analog LR PAM4 RX Design Challenges
Trend (50Gb/s ADC-Based PAM4 Transceiver)
Hybrid Equalization
Linear EQ - Reducing Peak to Main Ratio
ADC Requirement - can we use ENOB?
ADC Requirement for High Speed Link
Statistical Framework for ADC-Based Link
Example of ADC Model for T/D Simulation
Example: ADC Resolution vs BER
ADC BW, Linearity, Noise, Skew, Jitter
Asynchronous SAR-ADC Metastability
Error from Metastability vs Thermal Noise
PAM4 TX Design
Analog PAM4 TX
DAC-Based PAM4 TX
ADC-Based Receiver Block Diagram
RX Front-End Circuits
Inverter-Based CTLE
28GSa/s 32-Way Time-Interleaved ADC
ADC Sampling Front-End (SFE)
NMOS \u0026 PMOS Source Follower T/H Buffer
CMOS T/H Buffer
CMOS T/H Switch
Bootstrap T/H Switch
SFE Settling Time
SFE Pulse Response
Asynchronous SAR Sub-ADC
Sub-ADC 1-bit Conversion Timing
Sub-ADC Comparator
ADC Clocking
Skew Correction Circuit
ADC Circuit Verification/Simulation
RX Clocking - ILRO + CMOS PI
Outline
Digital Signal Processing (DSP) Block
DSP Block Diagram
ADC Gain \u0026 Offset Correction
FFE Multipliers \u0026 Adders
Digital Data/Error Slicer
1-tap Speculative DFE
DFE MUX
The CPU and Von Neumann Architecture - The CPU and Von Neumann Architecture by MrBrownCS 421,363 views 7 years ago 9 minutes, 23 seconds - Introducing the CPU, talking about its ALU, CU and register unit, the 3 main characteristics of the Von Neumann model, the system ...
Intro
CPU = Central Processing Unit
Von Neumann Architecture
Computers have a system clock which provides timing signals to synchronise circuits.
Fetch-Execute Cycle
CICC ES3-2 \"Optical Links\" - Prof. Azita Emami - CICC ES3-2 \"Optical Links\" - Prof. Azita Emami by IEEE Solid-State Circuits Society 7,614 views 4 years ago 1 hour, 31 minutes - Abstract: In this talk we will

focus on **design**, and analysis of high data rate receivers and transmitters for optical interconnects.
Intro
Outline • Motivation and introduction
Data Rates Scaling for Data Centers
Power Efficiency Challenge
Next-Gen Optical Links
Optical Links: Key Building Blocks
Photo-Detector
Photo-Diode Model
Optical Receiver: Resistive Front-end
Transimpedance Amplifier (TIA)
TIA Topologies
TIA with Shunt-Shunt Feedback
TIA Design Challenges
TIA Design in Scaled CMOS
Inverter-Based TIA Example
Effects of the Feedback Resistor (RF)
Co-design with Equalization
Look-Ahead Decision Feedback Equalizer
Alternative Receiver Front-Ends
Integrate-Reset Frontend
Double Sampling Integrating Frontend
Double Sampling Integrating Receiver
Revisit RC Front-end
RC Frontend and Double Sampling
Dynamic Offset Modulation
Modern SiP \u0026 3D Integration
Low-BW TIA with Feed-Forward Eq
CMOS SIP 3D Integration
Advanced Modulation Techniques
Multiplexing Transmission
Laser Diode Power Consumption
Motivation for APD
APD vs. PIN Photodiode
APD Advancement
APD-Based Optical Receiver Architecture
Modulation of Light
Integrated Optical Modulators
Phase Modulators
Amplitude Modulators
Micro-Ring Modulators (MRM)
Micro-Ring Modulators Challenges
Mach-Zehnder Modulators (MZM)
Travelling Wave Architecture
Modular Multi-Stage Driver
MOSCAP Drivers: Overview
Packaging Parasitics Co-Optimization
Modulator Parasitics Co-Optimization
Bandwidth Extension Technics
Preamplifier Chain Example
Micro-Ring Modulator (MRM) Drivers
Driver Design for Carrier Depletion MRM
AC-Coupled Differential MRM Driver

High-Voltage Output Stage
Optical Circuits for PAM4
CICC 2019 ES1-3 - \"Power Management for the Internet of Things\" - Patrick P. Mercier - CICC 2019 ES1-3 - \"Power Management for the Internet of Things\" - Patrick P. Mercier by IEEE Solid-State Circuits Society 6,493 views 4 years ago 1 hour, 37 minutes - Abstract: Small, ultra-low-power integrated **circuits**, afford new opportunities to sense and interact with the environment in new and ...
Intro
GROWTH OF THE IOT
Powering the internet of things
General trend in power management: size \u0026 efficiency
Trade-off between efficiency \u0026 power density
General DC-DC converter specifications for lot
Dynamic power range requirements for loT
Presentation Outline
Linear voltage regulator
Efficiency of linear regulation
Linear regulator: circuit implementation
Low drop-out (LDO) regulator
Linear regulation - summary
The road to better efficiency: switching DC-DC converters
Another way to think about it
Periodic Steady State Analysis
Switching converter basics
Continuous and discontinuous conduction modes
Discontinuous conduction mode: the preferred choice for lo
CMOS integration
Soft Switching
Zero current switching in a DCM buck converter
Energy-efficient manner to implement ZCS
Primary loss mechanisms
Direct buck and boost converters
Indirect converter. Inverting Buck-Boost
CMOS-compatible implementation
Buck-boost operating in buck or boost mode
Energy Harvesting Promise in loT
The Power of S-parameters for High Speed Digital Design - The Power of S-parameters for High Speed Digital Design by Keysight Design Software 19,933 views 9 years ago 1 hour, 3 minutes - This video describes the advantages and use of **S**,-parameters for High Speed **Digital Design**,. For more information: ...
Intro
Divide and Conquer
Agenda
Unlike Unilateral Transfer Functions, Bilateral Analog Circuits \"Talk Back\"
Two-port Z-parameters
1 Measure
EXERCISE: \"Be the test set\"
Congratulations! You Are a Test Set!
EXERCISE: \"Be the EDA tool\"
Sharable, IP Protected Models
Measure Y With Shorts
Y series R
It's Hard To Create Opens and Shorts At High Frequency
Measure Z Without Opens
Measure Y Without Shorts

Linear Combination of Vi a, b
Define ZR, a, b At Measurement Plane of Each Port
Two-port S-parameters
Congratulations! You Are a VNA!
Extra Credit... Prove That...
2 Use With Boundary Conditions
Example: Voltage Gain of Series R
Power Waves Are Measurement Friendly
Heavy Attenuation
VNAs Contain 3 or 4 Vector Voltmeters: Radio Receiver Architecture
What About High Frequency?
Voltage is Path Dependent
Multi-port Measurement
Single Ended to Differential Conversion
Modes and Signals
Bandlimited S-parameters in Time Domain Simulations (Eye Pattern)
Severe Case: Bandlimited Inverse Transform of Lossless Transmission Line
Forward Fourier Integral Built From Sinusoids
All Sinusoids Start at Minus Infinity
What Set of Sinusoids Can We Add to Make a Causal Impulse Response?
Kramers-Kronig Relation Provides the Recipe 1. All functions can be trivially decomposed into the sum of an even and an odd function.
Decompose any function, causal or not
signum function from sines (Odd)
So Now What?
Yes, But So What? • Imaginary part in freq comes from the odd part in time
Rao Method
How Far Can We Go With Electrical I/O? - How Far Can We Go With Electrical I/O? by ISSCC Videos 4,165 views 7 years ago 19 minutes - The demand for electrical links to supply increased bandwidth has continued to rise unabated despite that fact that underlying ...
Importance of Electrical Links
The Challenge Facing Electrical I/O
Electrical I/O Trends
The Bad News
Problem with Channel Loss
Fixing the Loss Problem
Cable Loss Characteristics
Circuit Limit: Amplifier Speed vs. Power
Circuit Power Limit
Summary
LC3 Interrupts - LC3 Interrupts by ECE290AMGroup 5,057 views 11 years ago 14 minutes, 9 seconds - ... saw on the module this is exactly how the **circuit**, functions the condition codes can be calculated using logic on the bus signal or ...
LC3 Control Unit Intro - LC3 Control Unit Intro by ECE290AMGroup 5,867 views 11 years ago 3 minutes, 45 seconds
HIGH SPEED SERDES (INTRODUCTION) - HIGH SPEED SERDES (INTRODUCTION) by Analog Layout \u0026 Design 67,360 views 4 years ago 25 minutes - This video discusses about High speed SERDES. Serial communication interface. Connectivity IP. It discusses at a very basic ...
Von Neumann Architecture - Computerphile - Von Neumann Architecture - Computerphile by Computerphile 642,903 views 6 years ago 16 minutes - Von Neumann Architecture is how nearly all computers are built, but who was John Von Neumann and where did the architecture ...
Von Neumann Architecture for Computers
Von Neumann Machine

CICC ES3-4 - \"Mixed-signal electrical interfaces\" - Prof. Elad Alon - CICC ES3-4 - \"Mixed-signal electrical interfaces\" - Prof. Elad Alon by IEEE Solid-State Circuits Society 17,575 views 4 years ago 1 hour, 28 minutes - Abstract: While some market segments have driven SerDes implementations towards DSP-heavy approaches, in many scenarios, ...
Intro
The SerDes Problem in a Nutshell
SerDes \"Golden\" Architecture (2005 - 2018+)
Didn't I Just Hear a Great Talk About ADC- Based Serdes?
Outline
Component #1: Digital Power
GBW-Limited Analog Power
Key Implication
Analog Pre-Processing Example: CTLE
Important Note
Equalization Architecture (2)
Key Challenges at 56/112G
Improving Efficiency: Current Integration
Current Integration Benefits In Detail
Common VGA Designs
Solution: Variable Bias Cascode VGA Transfer Function
(Analog) Parallelism
Switching Matrix Architecture
CDR Architecture: Dual Loop?
Oversampled vs. Baud-Rate CDR
Limitations of Classic Baud-Rate CDRs Mueller-Muller algorithm is most common
Avoiding Ambiguous Phase Integrate-reset front-end reshapes the pulse response to have a single peak point . This point corresponds to the equalized maximum voltage margin
Cursor Amplitude Estimation • Data-level (dLev) tracking loop (for eq, adaption) re- used to estimate cursor amplitude
Naïve Implementation Bandwidth
Improving CDR Bandwidth • User error sampler output instead of dLev • Find peak by intentionally dithering phase by A • Correlation of error and indicates phase error direction
Dither Path Delay Mismatch
week 1 assignment, digital circuit, | NPTEL | SWAYAM | - week 1 assignment, digital circuit, | NPTEL | SWAYAM | by engineerstechnic 120 views 3 years ago 1 minute, 7 seconds
Search filters
Keyboard shortcuts
Playback
General
Subtitles and closed captions
Spherical videos